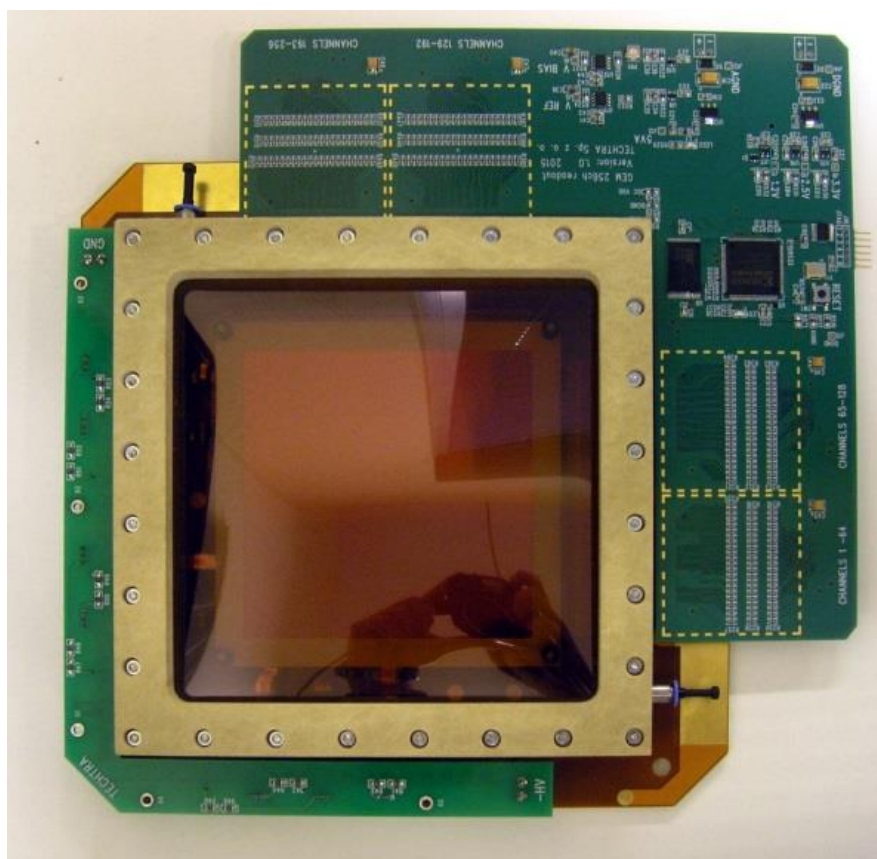# 256 channel readout board for 10x10 GEM detector

User's manual

This user's guide describes principles of operation, construction and use of 256 channel readout board for 10x10 cm GEM detectors. This manual also describes the protocols used and the accompanying PC software.

The readout board consist of four DDC264 current/charge-to-digital converters, an FPGA to control the device, and an Ethernet communication module for communication with PC. The Texas Instruments® DDC264 integrated circuits are 64-channels 16/20-bit analog to digital converters with current inputs (see more at TI DDC264 product page). The board is designed for operation with 10x10 cm standard CERN® GEM detectors and connects with to the detector using four Panasonic® connectors. This device is complete, ready to use, and has an easy to use PC software that makes it ideal for getting started with the GEM technology.

Contents

1. Theory of operation

This 256 channel readout board consist four DDC264 integrated circuits from Texas Instruments. Below is a description of these IC's taken from the Texas Instruments® DDC264EVM User's Guide[1]:

The DDC264 is a 20-bit, 64-channel, current-input analog-to-digital (A/D) converter (see Figure 1). It combines both current-to-voltage and A/D conversion so that 64 separate low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized. For each of the 64 inputs, the DDC264 uses the proven dual switched-integrator front-end. This design allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. Adjustable full-scale ranges from 12.5pC to 150pC and adjustable integration times from 160µs to 1s allow currents from fAs to µAs to be continuously measured with outstanding precision. Low-level linearity is ±1.0ppm of the full-scale range and noise is 6.3ppm of the full-scale range.

There are four different capacitor configurations available on-chip for both sides of every channel in the DDC264. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC264. The range control bits (Range[1:0]) set the capacitor value for all

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integrators. Consequently, all inputs and both sides of each input always have the same full-scale range. Table 1 shows the capacitor value selected for each range selection.

Table 1 RANGE SELECTION

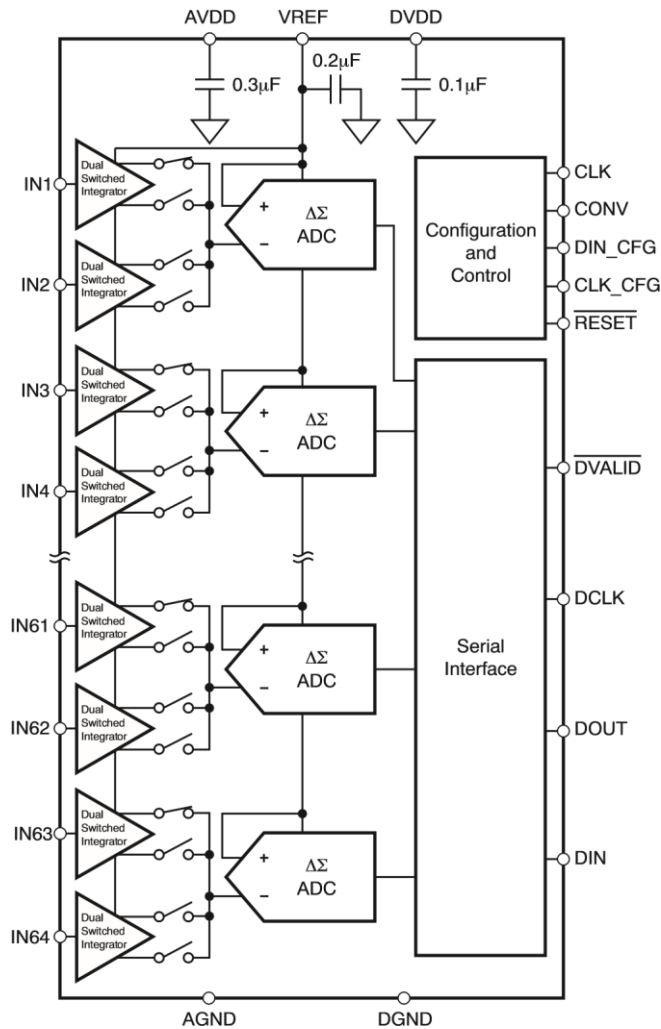| | Range Control Bits | | | |
Range	Range[1]	Range[0]	C_F	Input Range
0	0	0	3pF	−0.04 to 12.5pC
1	0	1	12.5pF	−0.2 to 50.0pC
2	1	0	25pF	−0.4 to 100pC
3	1	1	37.5pF	−0.6 to 150pC

Figure 1 DDC264 FUNCTIONAL BLOCK DIAGRAM

2. Hardware description

The 256 channel readout board for 10x10 cm GEM detectors consist of two separate parts – analog part and digital part.

The analog part consist of four DDC264 devices, a 4.096V reference with buffer, an adjustable current/charge bias circuit with an additional 4.096V reference and an analog power supply circuit.

The digital part contains a Xilinx Spartan™-3 FPGA, a communication module, a PROM memory with the FPGA configuration, an oscillator and a digital power supply circuit. The FPGA generates all of the timing clock signals for DDC264s, retrieves data from DDC264s, buffers the data and handles the communication between the DDC264s and the PC.

Under the main board there is connector for communication module. The communication board consist of 100 Mbit/s Ethernet controller, RJ-45 connector, oscillator and power supply. The readout board connects to a PC via RJ-45 connector accepts standard Ethernet cable. The Ethernet communication can be reset by pressing reset switch on the communication module board.

2.1   Power-Supply Circuit

There are two power supply connectors on the readout board. The J7 connector is the analog supply input, and the J8 is for the digital supply. The analog power supply consist of a 5 V regulator, decoupling capacitors, and reference and bias circuits. The digital power supply consist of a 5 V regulator on the input, decoupling capacitors and voltage regulators for the FPGA and DDC's. The digital voltages for FPGA and DDC's supply are regulated from 5 V to 3.3V, 2.5V, and 1.2V using three voltage regulators.

LEDs 2-5 that represent the required voltages should be lit when the readout board is powered correctly.

2.2   Reference and Bias Circuits

The 256 channels readout board uses two 4.096V references sources (REF3040) – one for the DDC integrated circuits reference, second for inputs bias circuit. Outputs of the references have been connected to a single pole low-pass-filters (3,386 Hz). After the filter reference voltage is followed by an amplifier configured as a buffer. In Bias circuit signal from filter passing through PR1 potentiometer which allows to change current/charge value injected to the DDC's inputs and after that bias voltage is followed by an amplifier configured as a buffer. Bias voltage is connected to the 100 MΩ resistors matrix, to inject the constant bias current/charge to all of the analog DDC's inputs, allowing them to work with negative signals coming from detector.

2.3   Switches and LED's

On the main board there are the LED indicators which allows to easily monitoring the board operational state. Refer to Table 2 for a summary of these indicators.

Table 2. LED Indicators Functions

LED	Color	Function
LED1	Green	FPGA configuration is done
LED2	Red	Analog 5 V is connected
LED3	Green	Digital 3.3 V is available
LED4	Green	Digital 2.5 V is available
LED5	Green	Digital 1.2 V is available
Link LED (on the RJ-45 conn.)	Green	Ethernet connection is established
RX/TX LED (on the RJ-45 conn.)	Yellow	Board is sending/receiving data to/from PC

Switch SW1 on the main board described as RESET, resets the FPGA. Normally, it should not be necessary to use this switch. Pressing this switch resets the FPGA to power-up conditions.

2.4   FPGA programming connector

The motherboard is equipped with 6-pins gold-pin type connector (J16) which allows to change FPGA software. Programming is carried out using standard JTAG protocol. Refer to Table 3 for the J16 JTAG connector specification.

Table 3 JTAG connector specification

PIN	Function
1	TMS
2	TDI
3	TDO
4	CLK
5	GND
6	3.3 V VDD

3. Low noise operation requirements

The 256 channel readout board for GEM detectors needs proper power supply and EMI shielding to ensure low-noise operation. Note that the digital part of the board is separate from the analog part. It is recommended to supply analog and digital part with separate, low noise voltage sources from linear laboratory power supply to avoid noise passing through from digital to analog part. The analog traces length between detector Panasonic® connectors and DDC integrated circuits are minimalized to reduce EMI noise coupling. All of the DDC256 IC's with current-limiting resistors are placed in a shielding cabinets.

Even though the 256 channel readout board is designed for optimal noise performance, it is necessary to close the detector with a readout board in a EMI shielding enclosure to eliminate any extraneous environmental noise sources.

4. Communication protocol

Four 64 channel ADCs (256 channels in total) with sampling rate of 4kSa/s gives high data rate. To ensure all data are collected properly and sent to the Ethernet network, FPGA was used. Figure 2 shows simplified schematic of data flow in GEM Detector board.
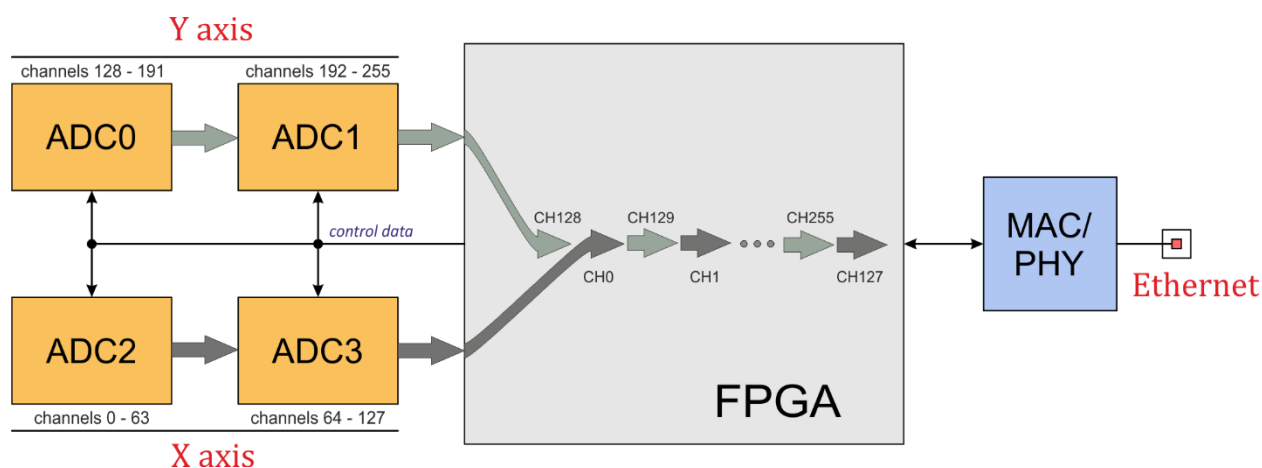

Figure 2 Simplified data flow schematic

To ensure both control of packets containing commands and high data throughput, the Techtra 256 channels readout board uses two communication protocols - TCP and UDP. The used communication protocols are described below.

4.1 Control protocol – TCP

TCP command set containing a description of the commands that are sent to the detector with answers from the detector are described in Table 4.

Table 4 Command set

	Command	Description	Answer	Comment
1	0x00	ID acquire	Detector's ID	"TECHTRA 256Ch GEM Detector V:1.0 SN:XXXX" ASCII coded, 20 bytes total
2	0x01	Firmware version	Firmware version	b00000001xxxyyyyy version: x.y in binary 2 bytes total command length
3	0x02 + [range]	DDC range set	0xFF	[range]: 000000xx, xx: 00 – 3 pC 01 – 12,5 pC 10 – 25 pC 11 – 37,5 pC 2 bytes total command length
4	0x03 + x00[time]	Integration time set	0xFF	Where [time] is number equal to ((time in ns)/12,5 ns - 1) written on 28 bits Count range: (13279 : 79999999) 5 bytes total command length
5	0x04	Constant measurements trigger	0xFF	
6	0x05	Single measurement trigger	0xFF	
7	0x06	Measurements stop	0xFF	
8	0x07	Keep alive	0xFF	Simple answer if connection is present

4.2   Data protocol – UDP

Each pair of ADCs is connected together in Daisy-Chain giving a serial interface with 128 channels. FPGA controls the integration time intervals and acquires the data from both Daisy-chains simultaneously. To prepare a UDP packet, two streams are interlaced together. DDC264s output the data from the oldest channels, so resultative stream is a mix beginning with 127, 255, 126, 254, downwards.

The UDP packet structure has been described in Table 5. Figure 3 shows a sample of data stream in UDP packet.

Table 5 UDP packet structure

Data type	Frame numer	Data
Size	4 Bytes	256 x 3 B, 768 Bytes total
Comment	starting from 0 on each power-on	order: 127 – 255 – 126 – 254 - … - 0 – 128 structure: x0nnnnn, where n – measured data

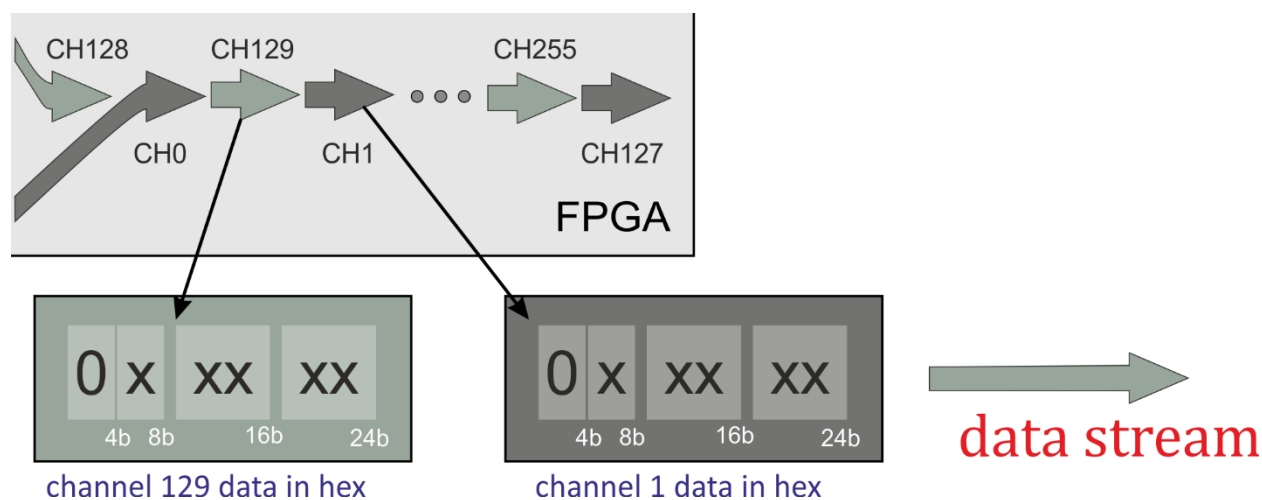channel 129 data in hex   channel 1 data in hex

data stream

Figure 3 Data stream structure

5. PC application

The 256 channels readout board for GEM detectors uses Ethernet connection for communication with PC. It is preferred to connect the readout board with a PC using separate 100 Mbit/s Ethernet card, to ensure proper working of the device and that no data will be lost.

To establish a connection between detector and PC, it is necessary to setup network adapter correctly. Figure 4 shows how to correctly set up a Ethernet adapter on Microsoft® Windows® system. Please refer to the detector's individual parameters sheet for proper IP addresses.
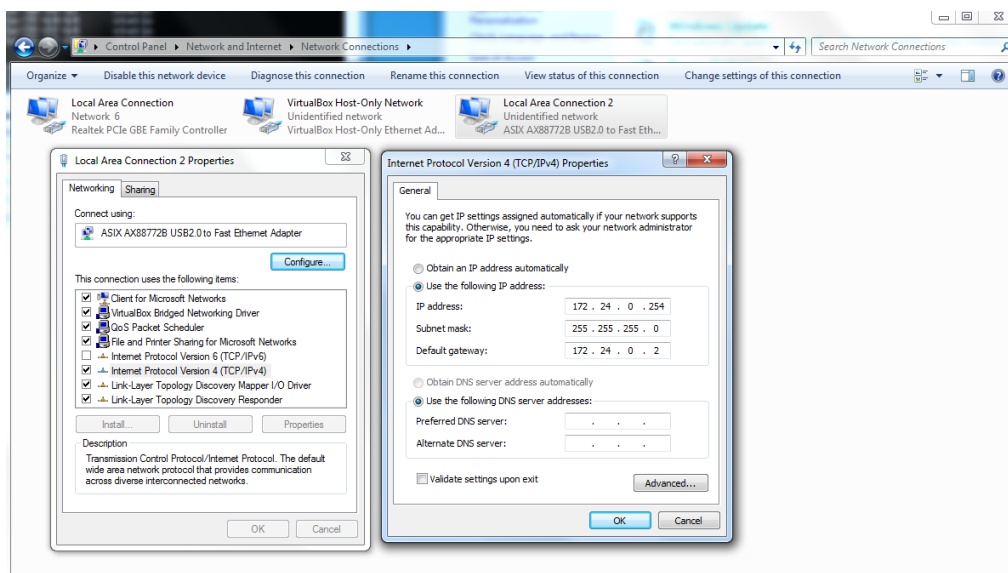

Figure 4 How to proper setup the Ethernet adapter on PC computer with Microsoft® Windows®

To ensure that PC application will be able to connect to the detector it is needed to allow access through Windows® firewall – see Figure 5.
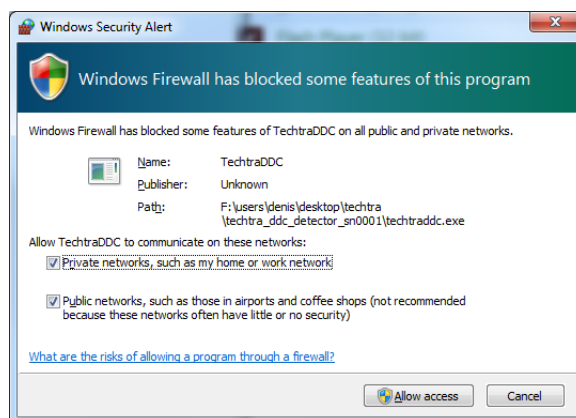

Figure 5 Allowing to access through Windows® firewall

After the application startup, the main window should appear. Figure 6 shows the application before (a) and after (b) connection established. The application at startup opening the connection and waiting for new client (detector readout board). Detector automatically send SYN packets to open the connection. The connection between PC and detector should be established in less than 1 minute.

If after 1 minute application won't connect, than please check if:

1. Power supply for the detector is turned on,
2. Ethernet cable is properly connected to the detector,
3. Ethernet IP configuration is done properly,
4. Application isn't blocked by firewall,
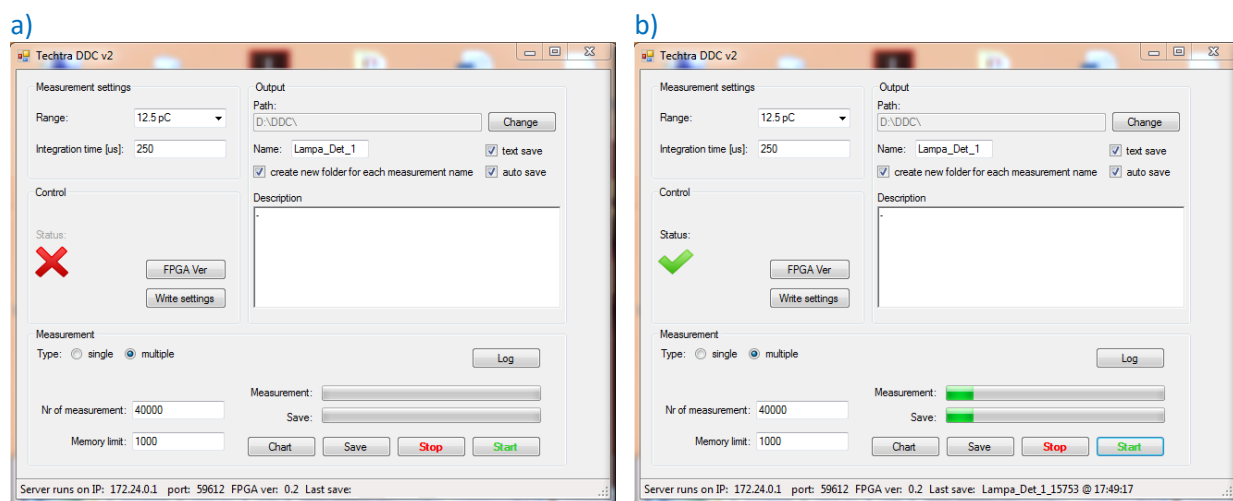5. Application's configuration contains the actual IP address of the detector.

Figure 6 PC application main window showing Ethernet communication status: a) unconnected, b) connected

The application controls were divided into several blocks: Measurement setup, Control, Output and Measurement. The measurement setup consist of user defined DDC range and single measurement integration time. In a control section there are: button for FPGA version read-back, button for write settings into FPGA (settings are also automatically written when a measurement is starting), and connection status indicator. The output section consist of user defined path for measurement saving, File name for measurements, checkbox for making a new folder for each measurement series name, checkbox for choosing file format (binary if unchecked, text if checked), and checkbox for saving measurement data to file (or not if unchecked). The measurement section consist of: type of measurements (single or multiple), number of measurements, memory limit for measurements buffering, button for Log window, button for window with charts, Start/Stop buttons and progress bars for measurements and saving to the files.

Figure **7** shows the PC application with all windows opened (main window, log window and charts window). Charts window consist of two charts: candlestick plot for all channels on the top and channel line plot for one chosen channel. The channel for the line plot can be selected using the "Channel nr" control. Charts can be auto-scaling and auto-updating or manual updating using "Update" button.
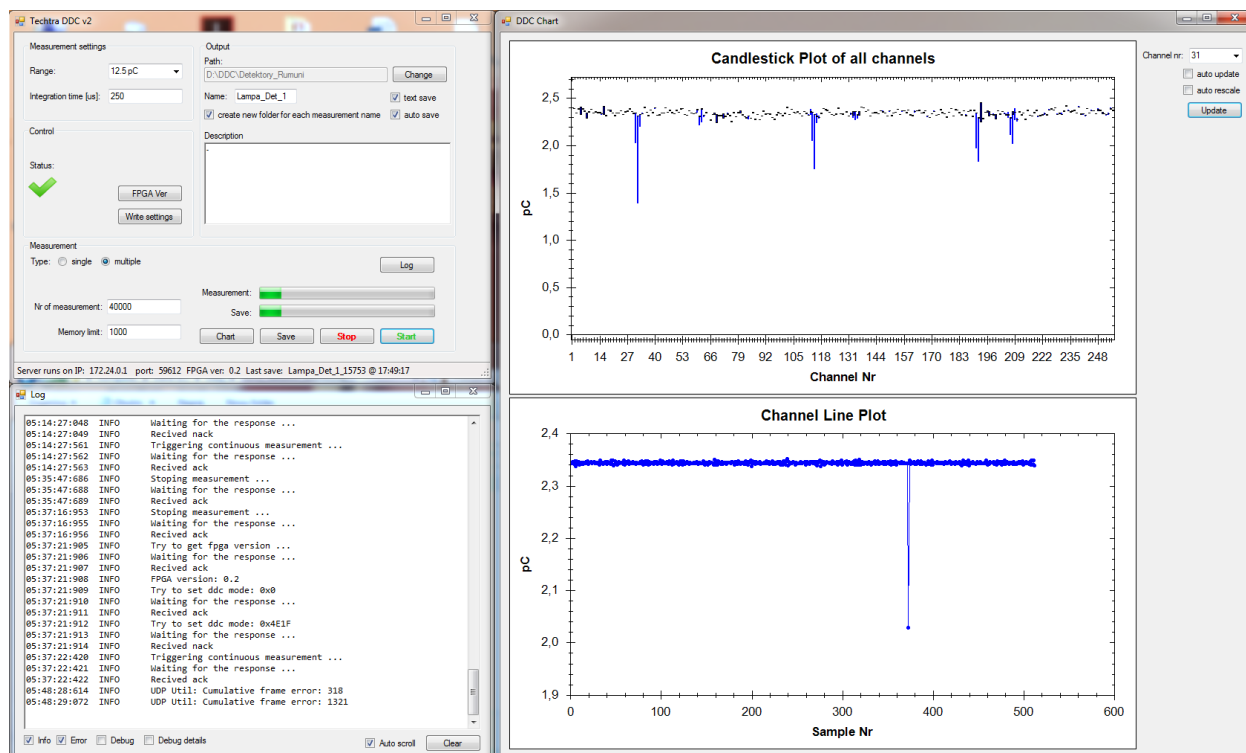

Figure 7 PC application with all windows opened

Obtained data is being saved to two different type of files: text or binary. The former usually requires a bit more disk space but it can be easily analyzed the latter was designed to achieve best save performance and lowest disk usage. Save process can be triggered automatically by software (if the auto save checkbox is checked) or manually by user (using save button).

Files are saved using following name convention: measurmentName_index.dat where name can be set in user interface and index is automatically set by software. New folder can be created by software for each new measurement name (if the proper option in chosen).

Text file consists of two part: header and data matrix. Header includes: basic measurement settings (DDC range and integration time) and data provided by user (name, description).

Exemplary text file header:

#-------------DDC Params-------------#

Range = 150 pC

Integration time = 160

##------------Other------------------##

Name: name

Description:

desc

Data matrix begins with two lines. The first line contains numbers in sequence, each number corresponds to sample No. The second line provides information about time interval between data samples - "1" means that data is consistent and data loss didn't occur. The higher number e.g. "3" means that two samples were lost during transmission (it means that time interval between samples is three times bigger). After those lines start NxM data matrix. N is fixed size (256) and it's defined by number of channels. M can vary and depends on container size. Data structure in file is as follows:

$$\begin{bmatrix} c_0 s_0 & \cdots & c_0 s_{M-1} \\ \vdots & \ddots & \vdots \\ c_{N-1} s_0 & \cdots & c_{N-1} s_{M-1} \end{bmatrix}$$

$c_N s_M - channel\ \boldsymbol{n}\ sample\ \boldsymbol{m}$

Software uses default system decimal mark (most European countries ","). Data samples are separated by tabulator "\t". Each row is ended by new line mark. Binary file specification has been described in Table 6.

Table 6 Binary file specification

Position	Type	Name	Description
1	B	Range	0 to 3 value corresponding to DDC range (see datasheet)
2	UINT	Integration time	Time in µs
3	UINT	Channel number	Number of channels - in current hardware solution - 256
4	UINT	Sample number	Number of samples obtained for single channel
5	UINT	dt	Sample number-1 values corresponding to time different between samples (as in text file)
6	DOUBLE	Data matrix	-

Data alignment is the same as in text format file (see data matrix) but samples are not separated by tabulator. Binary types definition has been described in Table 7.

Table 7 Binary types definition

Type	Description
B	8 bit unsigned integer
UINT	32 bit unsigned integer
DOUBLE	double-precision floating point format - 64 bit