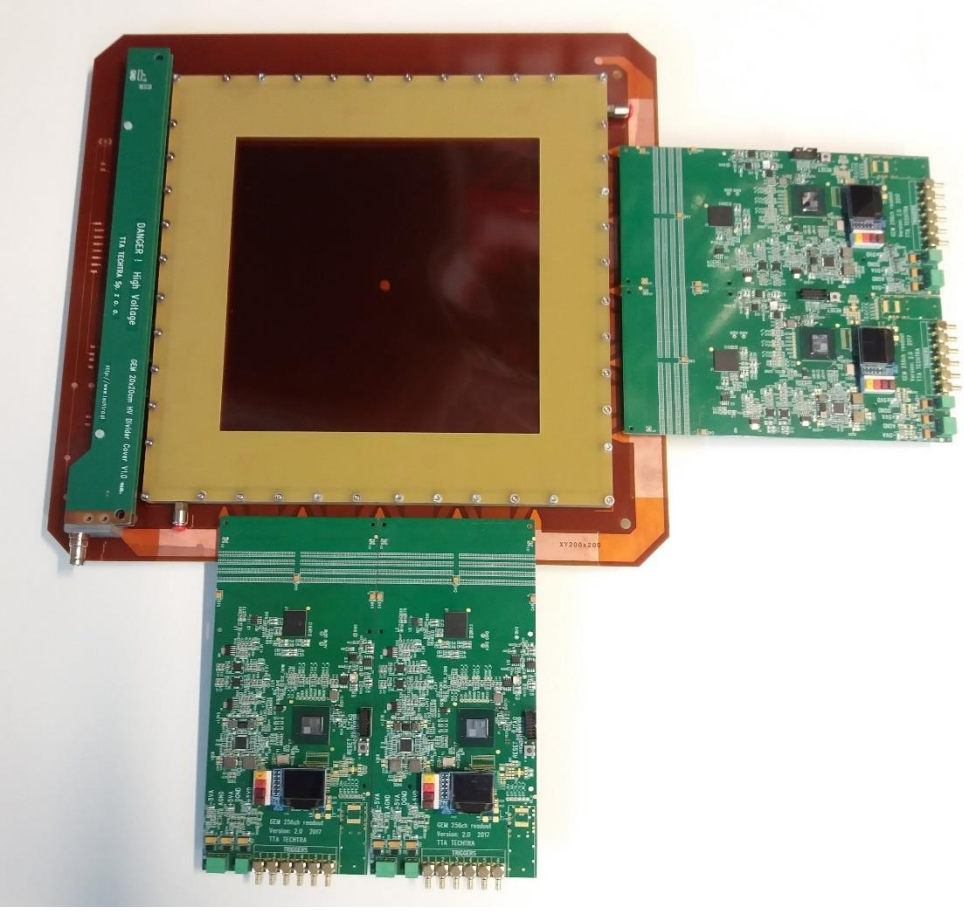
256 channel readout board V2.0 for GEM detector

User's manual



This user's guide describes principles of operation, construction, and use of 256 channel readout board for GEM detectors. This manual also describes the protocols used and the accompanying PC software.

The readout board consists of DDC2256A current/charge-to-digital converter, an FPGA to control the device, and an Ethernet communication module for communication with PC. The Texas Instruments® DDC2256A integrated circuits are 256-channels 24-bit analog to digital converters with current inputs (see more at TI DDC2256A product page). The board is designed for operation with any standard CERN® GEM detectors and connects with the detector via four

Panasonic® connectors. This device is complete, ready to use, and has easy-to-use PC software that makes it ideal for getting started with the GEM technology.

Contents

1. Theory of operation

This 256 channel readout board uses DDC2256A integrated circuit from Texas Instruments. Below is a description of these ICs from the Texas Instruments® DDC2256A Datasheet[1]:

"The DDC2256A is a 24-bit, 256-channel, current-input analog-to-digital A/D) converter. It combines both current-to-voltage integration and A/D conversion, so that 256 individual low-level current output devices, such as photodiodes, can be directly connected to their inputs and digitized in parallel (simultaneously).

[1] DDC2256A Datasheet, Texas Instruments, http://www.ti.com/lit/ds/symlink/ddc2256a.pdf, accesed december 2021

For each of the inputs, the DDC2256A has one low noise/low power integrator designed to capture the entire charge from the sensor. The integration time is adjustable from 58.8 µs to 100 ms, allowing currents from fA to µA to be continuously measured with outstanding precision. The outputs of the integrators are digitized by sixteen 24-bit low-power ADCs and all the resulting data is output over a single LVDS serial interface pair designed to minimize noise coupling in environments with high channel count.

The DDC2256A operates from a ±2.5-V analog supply, 1.8-V analog supply (AVDD_18), and 1.8-V digital supply (DVDD). The device is specified from 0°C to 70°C operating temperature and available in a 14 x 16 mm^2 323-ball 0.8 mm-pitch BGA. Finally, onboard reference buffer and bypass capacitors help to minimize the external component requirements and further reduce board space."

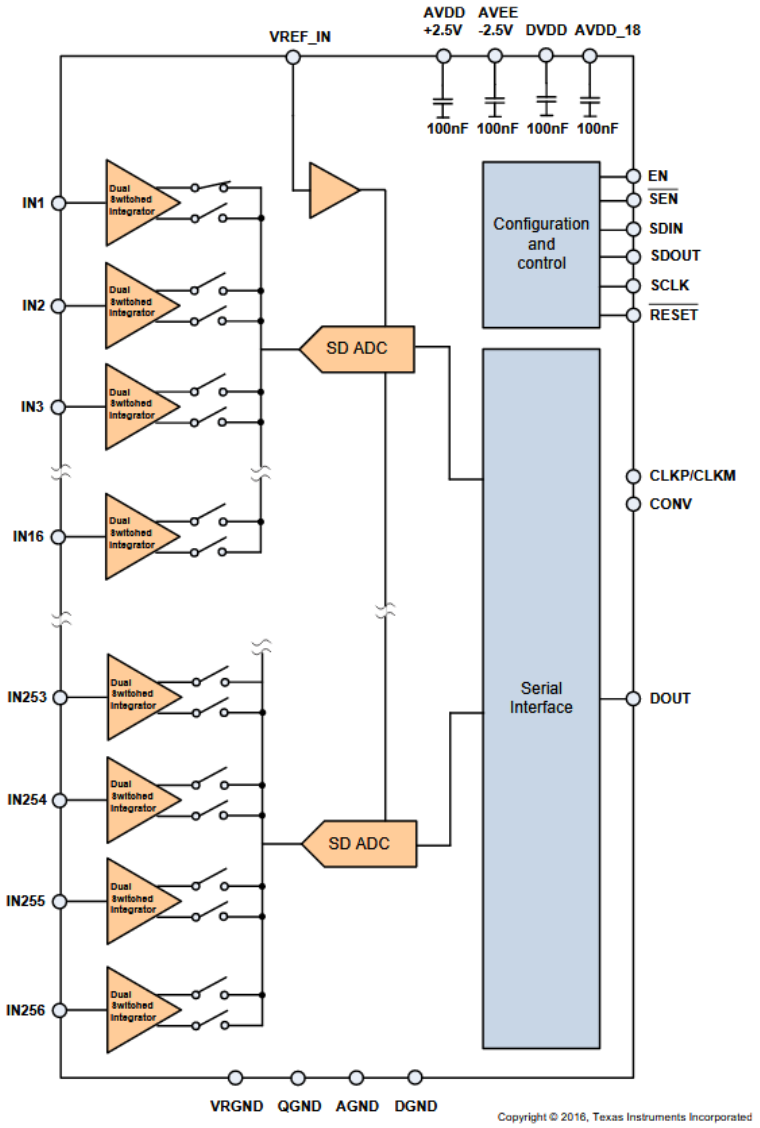


Figure 1 DDC264 FUNCTIONAL BLOCK DIAGRAM

2. Hardware description

The 256 channel readout board V2.0 for GEM detectors consists of two separate parts – the analog part and the digital part. The top view of the board is shown in **Figure 2**, wherein the bottom view is shown in **Figure 3**.

The analog part consists of a DDC2256A device, a 2.048V voltage reference with buffer, an adjustable current/charge bias circuit with an additional 2.048V voltage reference, and an analog power supply circuit.

The digital part contains a Xilinx Artix™-7 FPGA, a communication module, a PROM memory with an FPGA configuration, an oscillator, OLED display, EEPROM memory, configuration switches, Trigger I/O, and a digital power supply circuit. The FPGA generates all of the timing clock signals for DDC2256A, retrieves data from DDC, buffers the data, and handles the communication between a DDC and a PC.

On the bottom side, there is a socket for the communication module. The communication module consists of a 100 Mbit/s Ethernet controller, RJ-45 connector, oscillator, and power supply. The readout board communicates with a PC via RJ-45 and standard Ethernet cable.

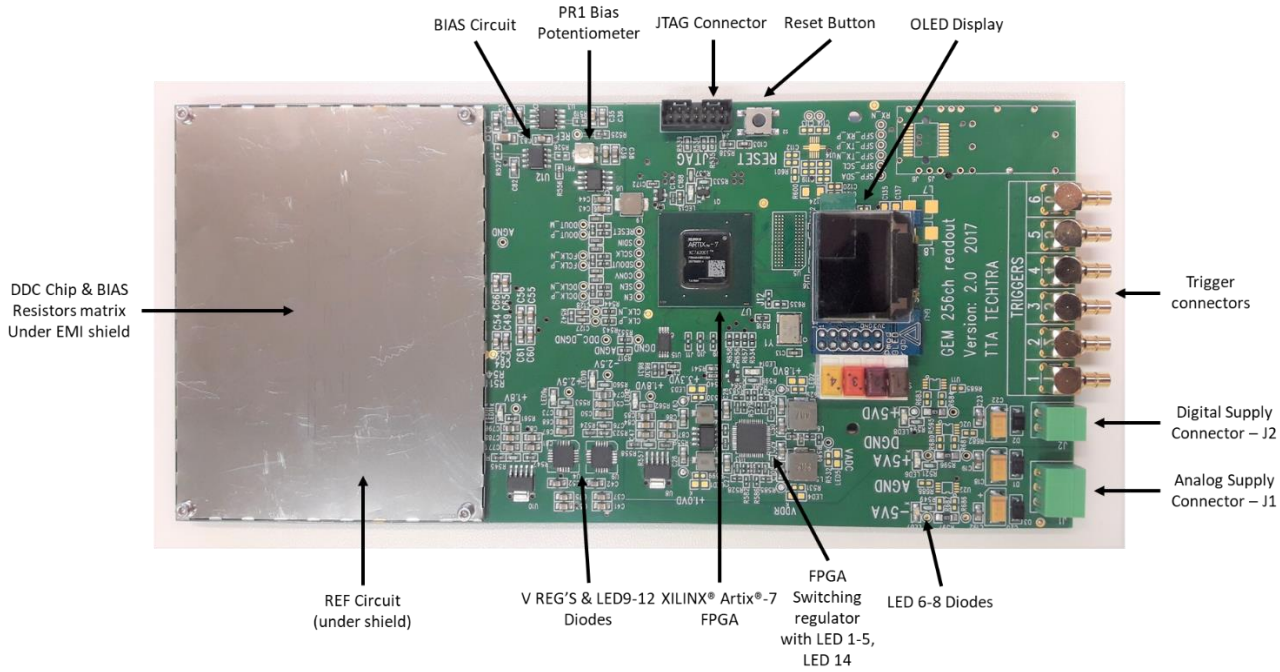


Figure 2 Techtra 256ch readout board V2.0 top view

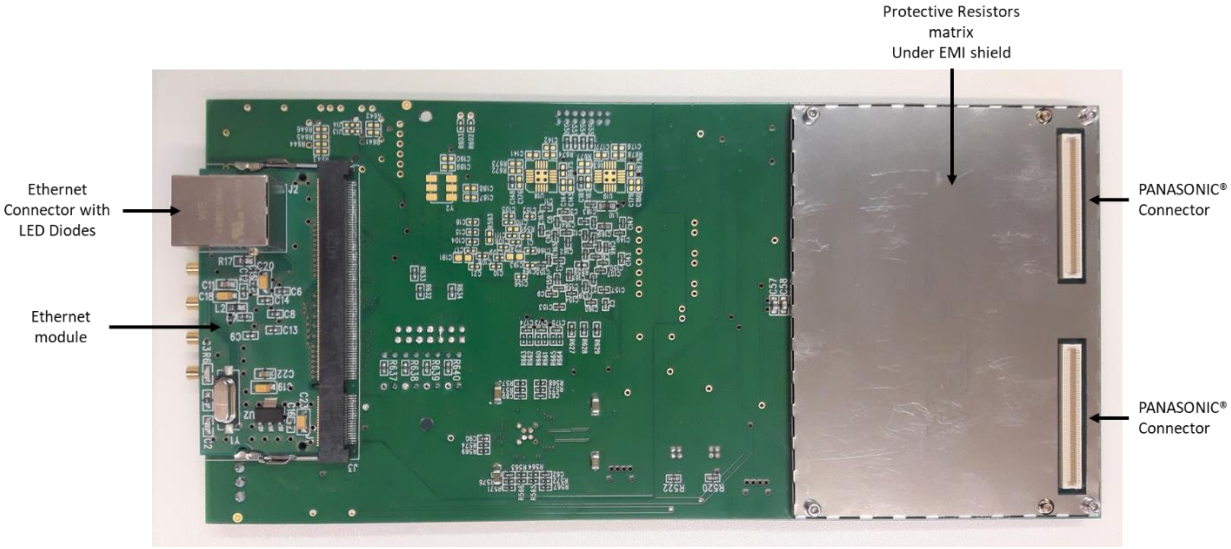


Figure 3 Techtra 256ch readout board V2.0 bottom view

2.1 Power-Supply Circuit

There are two power supply connectors on the readout board. The J1 connector is the analog supply input, and the J2 is for the digital supply. **We recommend using three separate DC low-noise Power Supply voltages – This ensures the best noise performance of the detector.** It is possible to use +5 V from J1 (analog supply connector) to power the digital part, but it will introduce additional digital noise. **The nominal supply voltage is +/-5 V DC for analog and +5 V DC for the digital section**, although it can be set in a range from 5 V to 9V. The power consumption for the analog section is 100 mA for the negative voltage and 200mA for positive. The power consumption of the digital part is 500 mA.

The analog power supply consists of +/-2.5 V regulators, +1.8 V regulator, decoupling capacitors, reference and bias circuits. The digital power supply consists of a linear +1.8 V regulator (DDC digital voltage), FPGA switching converter decoupling capacitors, and voltage regulators for the FPGA and DDCs. The digital voltages for FPGA are regulated from input voltage to: 3.3 V, 1.5 V (DDR), 1.8 V, 1.8 (ADC), and 1.0 V by four switching voltage regulators + a linear regulator for ADC.

LEDs 1-12 that represent the required voltages should be lit when the readout board is powered correctly.

2.2 OLED Display

Techtra 256ch readout board V2.0 is equipped with 96 x 64 px. OLED display. When the connection with PC software is not established, the display shows a complete IP config (Detector IP, Subnet Mask, TCP Port, UDP port, destination IP). When the connection is on, it shows the DDC range value and detector status (Connected, Sample, Oscilloscope). The display is useful to set up an Ethernet connection and to check detector status.

2.3 Reference and Bias Circuits

The 256 channels readout board uses two 4.096 V reference sources (REF3040) – one for the DDC integrated circuits reference the second for the inputs bias circuit. Outputs of these references have been connected to single-pole low-pass filters (3,386 Hz). After the filter reference voltage is followed by an amplifier configured as a buffer. In Bias circuit signal from filter passing through PR1 potentiometer which allows changing current/charge value injected to the DDC's inputs and after that bias voltage is followed by an amplifier configured as a buffer. **V2.0 detector contains a precise digital potentiometer that allows changing Bias current using PC software**. The bias voltage is connected to the 100 MΩ resistors matrix to inject the constant bias current/charge to all of the analog DDC's inputs, allowing them to work with negative signals from the detector.

2.4 Switches and LED's

On the mainboard, there are LED indicators that allow monitoring of the board's operational state. Refer to **Table 1** for a summary of these indicators.

Table 1 LED Indicators Functions

LED	Color	Function
LED1	Green	Digital 1.0 V is available
LED2	Green	Digital 1.8 V is available
LED3	Green	Digital 3.3 V is available
LED4	Green	Digital 1.5 V DDR is available
LED5	Green	Digital 1.8 V ADC is available
LED6	Red	Analog + 5 V is connected
LED7	Blue	Analog - 5 V is connected
LED8	Green	Digital + 5 V is connected
LED9	Red	Analog + 2.5 V DDC is available
LED10	Blue	Analog - 2.5 V DDC is available
LED11	Red	Analog + 1.8 V DDC is available
LED12	Green	Digital 1.8 V DDC is available
LED13	Green	FPGA configuration is done
LED14	Green	Power Good is OK
Link LED (on the RJ-45 conn.)	Green	Ethernet connection is established
RX/TX LED (on the RJ-45 conn.)	Yellow	Board is sending/receiving data to/from PC

Switch SW1 on the mainboard described as RESET, resets the FPGA. Normally, it should not be necessary to use this switch. Pressing this switch resets the FPGA to power-up conditions

2.5 FPGA programming connector

The motherboard is equipped with 14-pins 2 mm pitch MX connector (J4), which allows changing FPGA software. Programming is carried out with standard JTAG protocol. Refer to **Table 2** for the J16 JTAG connector specification.

Table 2 JTAG connector specification

Function	PIN	PIN	Function
GND	**1**	**2**	VREF
GND	**3**	**4**	TMS
GND	**5**	**6**	TCK
GND	**7**	**8**	TDO
GND	**9**	**10**	TDI
GND	**11**	**12**	NC
GND	**13**	**14**	NC

2.6 External Trigger interface

The electronic readout board includes six external trigger signal connectors. First four connectors are differential pairs, and the two last connectors are single-ended. The type of trigger signal (and corresponding connectors) can be chosen in the PC application. All signals are 3,3 V CMOS standard inputs or outputs. SMB connectors are used. The functions of these connectors are described in **Table 3**.

Table 3 Trigger inputs/outputs specification

Number	Name	Function
1	TRIG_OUT_DIFF_P	Trigger output differential signal pair
2	TRIG_OUT_DIFF_N	
3	TRIG_IN_DIFF_P	Trigger input differential signal pair
4	TRIG_IN_DIFF_N	
5	TRIG_OUT_SE	Trigger output single-ended signal
6	TRIG_IN_SE	Trigger input single-ended signal

2.7 Configuration switches

The detector board includes four color-coded microswitches that can be operated by the user. The functions of these switches are described in **Table 4**.

Table 4 Configuration switches specification

Number	Function
1	[OFF] – Normal operation, [ON] – Ethernet configuration mode.
2	Reserved
3	Reserved
4	Reserved

3. Low noise operation requirements

The 256 channel readout board for GEM detectors needs a proper power supply and EMI shielding to ensure low-noise operation. Note that the digital part of the board is separate from the analog part. It is recommended to supply analog and digital parts with separate, low noise voltage sources from linear laboratory power supply to avoid noise passing through from digital to analog part. The analog traces length between detector Panasonic® connectors and DDC integrated circuits are minimalized to reduce EMI noise coupling. All of the DDC256 ICs with current-limiting resistors are placed in shielding cabinets.

Even though the 256 channel readout board is designed for optimal noise performance, it is necessary to close the detector with a readout board in an EMI shielding enclosure to eliminate any extraneous environmental noise sources.

4. Communication protocol

256 channel ADC with a sampling rate of 17kSa/s gives a high data rate. To ensure all data were collected properly and sent to the Ethernet network, FPGA was used. Figure 4 shows a simplified schematic of data flow in the GEM Detector board. **In the V2.0 version, two more data processing methods were added – DSP and Oscilloscope.** The standard method is continuous signals measurement and sending the data to PC.

In **Oscilloscope mode**, the detector constantly measures data but doesn't send it to the PC. After receiving the trigger signal, the board sends to PC 256 samples measured before the trigger signal and 256 samples after the trigger occurs. In this mode, we see only the data acquired in the neighbourhood of the trigger signal.

In **DSP mode**, the readout is automatically processing the data to detect the peaks. The algorithm compensates Bias for each channel separately and detects channels on which signal is below the threshold value. After detecting the peak, FPGA process raw data to find peak location and total charge. In this mode, only calculated peak data are transferred to PC - this greatly reduces the data amount that is sent to PC.

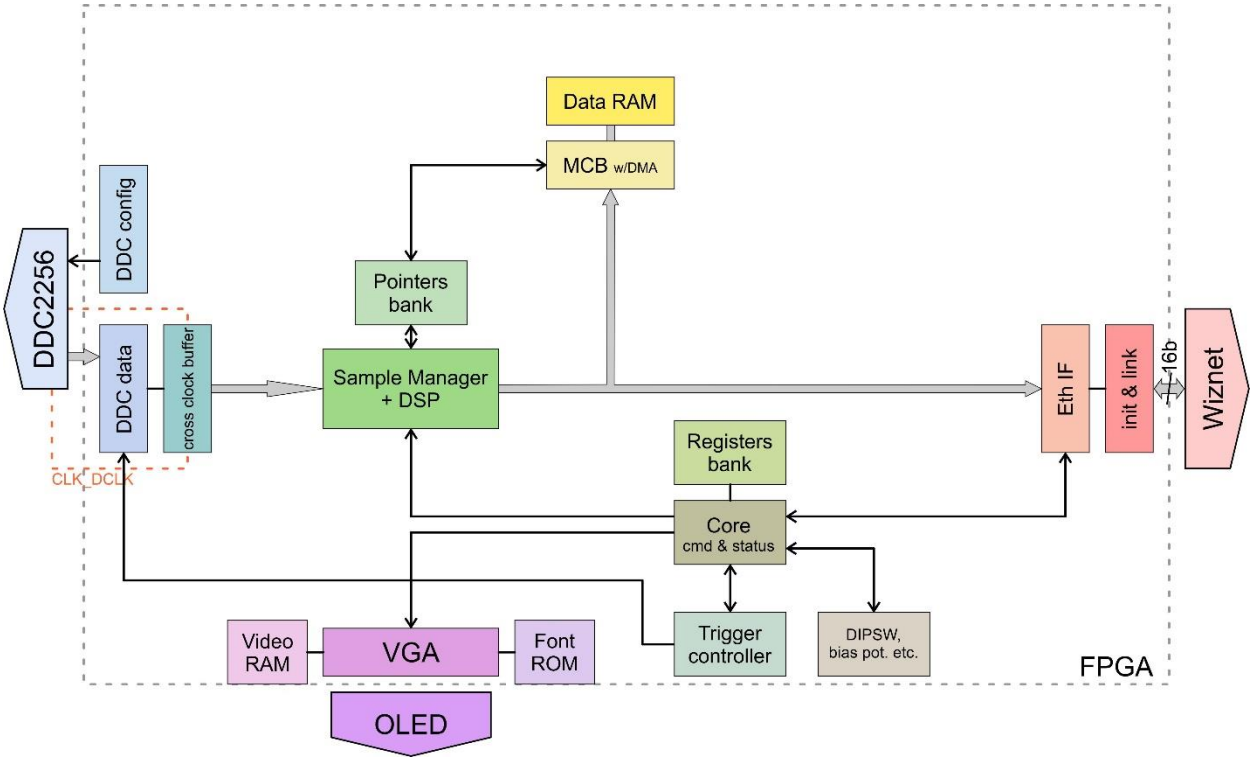


Figure 4 Simplified data flow schematic

To ensure both control of packets containing commands and high data throughput, the Techtra 256 channels readout board uses two communication protocols - TCP and UDP. The used communication protocols are described below.

4.1 Control Protocol – TCP

TCP command set containing a description of the commands that are sent to the detector with answers from the detector are described in **Table 5**.

Table 5 Command set

	Command	Description	Answer	Comment
1	0x00	ID acquire	Detector's ID	"TECHTRA 256Ch GEM Detector V:1.0 SN:XXXX" ASCII coded, 20 bytes total answer length
2	0x01	Firmware version	Firmware version	Answer structure: b00000001xxxyyyyy version: x.y in binary 2 bytes total answer length
3	0x07	Keep-alive	0xFF	Simple answer if the connection is present
4	0x10 + x00[config]	DDC Integration time set	0xFF	[config]: [B1] – Measurement mode: 000 – OFF 001 – Single measurement 010 – Multiple measurements 100 – Oscilloscope mode [B2] – Trigger: 1000 – Differential output trigger [ON] 0100 – Differential input trigger [ON] 0010 – Single-ended output trigger [ON] 0001 – Single-ended input trigger [ON] [B3- B6] – Integration time: Where integration time is the number equal to ((time in ns)/12.5 ns) written on 32 bits Count range: (4 804 : 8 000 000)

				7 bytes total command length
5	0x20 + [range]	DDC range set	0xFF	[range]: [b7] – "1" for integration time < 78 µs [b2- b0] – DDC range: 101 – 150 pC 000 – 100 pC 110 – 75 pC 001 – 50 pC 111 – 37. 5pC 010 – 25 pC 011 – 12.5 pC 100 – 6.25 pC 2 bytes total command length
6	0x30 + [bias]	DAC BIAS set	0xFF	[bias]: [b15- b12] – DAC settings [0101] [b11-b0] – DAC Value 3 bytes total command length
7	0x50 + [DSP]	DPS settings	0xFF	[DSP]: [B1] – DSP on [ON = 0b10000000], [OFF = 0x00] [B2- B4] – Trigger threshold [B5] – Peak neighborhood [B6- B8] – IQD threshold 9 bytes total command length
8	0xAA + [ip_config]	IP config settings	0xFF	[ip_config]: [B1- B4] – GEM IP [B5- B8] – Destination IP [B9- B12] – Subnet mask [B13- B14] – TCP port [B15- B16] – UDP port 17 bytes total command length

4.2 Data protocol – UDP

The 256 channel readout board V2.0 can work in one of three modes: Standard, Oscilloscope, and DSP. The two first modes are similar (data format is the same), so they both use the same UDP frame protocol.

The UDP packet structure in Standard and Oscilloscope mode has been described in **Table 6**. In this mode, the detector sends a packet with frame number and data from all 256 channels (from 0 to 255).

In DSP mode, the amount of data is significantly reduced, and the information structure is different, so it needs a different protocol. The UDP packet structure in DSP mode has been described in **Table 7**. The detector sends frame number, peak charge sum, peak barycenter, and ADC frame number.

Table 6 UDP packet structure in Standard and Oscilloscope mode

Packet bytes	775-772	771-768	767-0
Data	Frame number (4 Bytes)	[b771]: "0" when DSP is OFF	ADC data: (256 channels x 3 Bytes, 768 Bytes total)
Comment	starting from 0 on each power-on		order: from channel 0 to channel 225 structure: x0nnnnn, where n – measured data

Table 7 UDP packet structure in DSP mode

Packet bytes	19-16	15-12	11-8	7-2	1-0
Data	Frame number (4 Bytes)	[b15]: "1" when DSP is ON	Charge Sum (4 Bytes)	5x '0' & 43 bit Peak Barycenter	7x '0' & 9 bit Frame Number
Comment	starting from 0 on each power-on			Multiplied by 1024	ADC frame number

5. PC software – data acquisition

The 256 channels readout board for GEM detectors uses an Ethernet connection for communication with PC. It is recommended to connect the readout board with a PC using a separate 100 Mbit/s Ethernet card to ensure proper working of the device and no data loss.

To establish a connection between the detector and a PC, it is necessary to set up a network adapter correctly. **Figure 5** shows how to correctly set up an Ethernet adapter on the Microsoft® Windows® system. **Please refer to the detector's individual parameters sheet for proper IP addresses.**

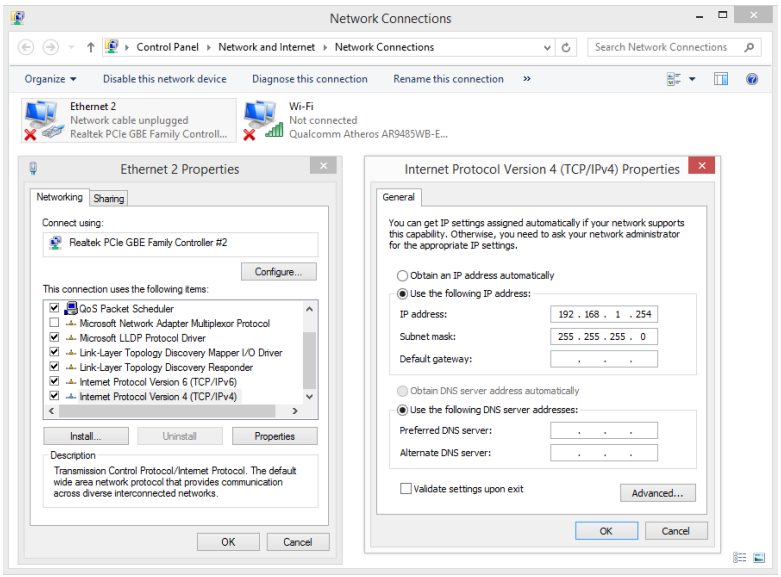


Figure 5 How to properly set up the Ethernet adapter on a PC with Microsoft® Windows®

To ensure that the PC application can connect to the detector, it is needed to set access through Windows® firewall – see **Figure 6**.

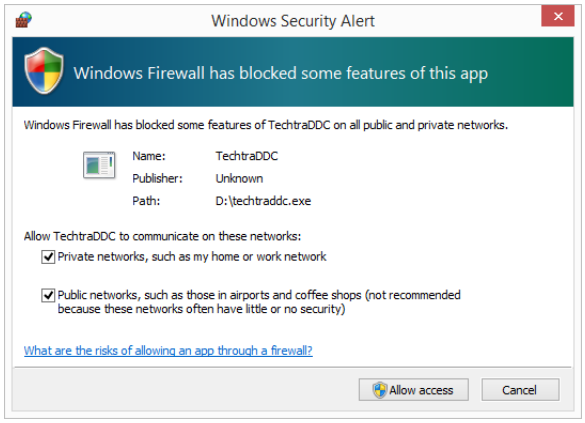


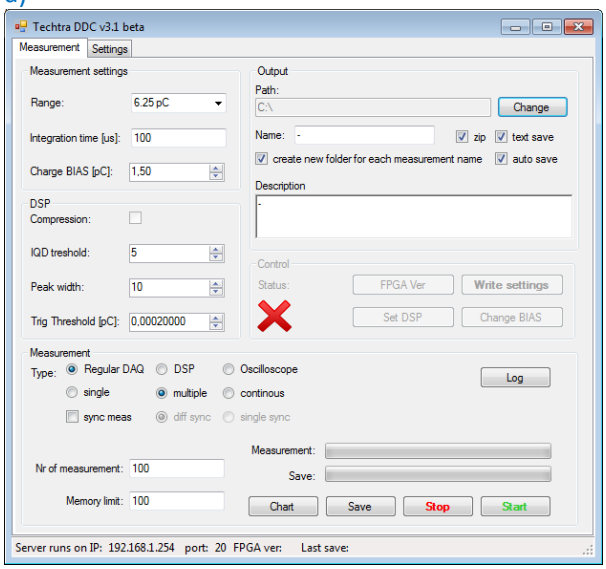
Figure 6 Setting the access through Windows® firewall

On the application startup, the main window should appear. **Figure 7** shows the application before (a) and after (b) connection is established. The application at startup opens the connection and waits for a new client (detector readout board). The detector automatically sends SYN packets to open the connection. The connection between PC and detector should be established in less than 1 minute.

If after one-minute application will not connect, then please check if:

1. The power supply for the detector is on,
2. Ethernet cable is correctly connected to the detector,
3. Ethernet IP configuration is done correctly,
4. Application isn't blocked by the firewall,
5. The application's configuration contains the actual IP address of the detector.

a)



b)

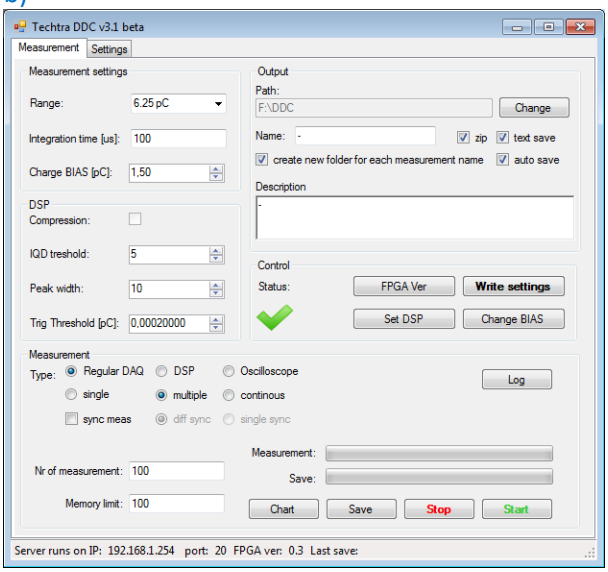


Figure 7 Data acquisition software V3.1 main window showing Ethernet communication status: a) unconnected, b) all readout boards are connected

Techtra DDC application V3.1 is designed for data acquisition from DDC V2.0 readout – it's not backward compatible with V1.0 and V1.1 detectors. In the main window, there are two tabs: Measurement (main tab) and Settings. The application controls on the Measurement tab are divided into several blocks: Measurement settings, DSP, Measurement, Control, and Output.

The measurement settings consist of user-defined DDC range, single measurement integration time, and Bias charge value. **Bias charge should be set to at least half of the DDC range – In another way, the charge values measured by the detector can be wrong.**

In the DSP section, there are user-defined DSP parameters such as IQD threshold, Peak width, and Trig threshold. In this mode, there are two threshold methods – using noise level of each channel multiplied by IQD threshold value (trigger depends on noise level), or standard method using predefined value defined by Trig Threshold parameter. Detector uses larger of these values as the threshold. The peak width parameter determines the number of channels from both sides of the peak center, which charge is summed to the total charge.

The measurement section consists of measurement mode (Regular DAQ, DSP, or Oscilloscope), type of measurements (single, multiple, or continuous), sync checkbox with two parameters (diff sync or single sync), number of measurements, memory limit for measurements buffering, a button for Log window, a button for window with charts, Start/Stop buttons and progress bars for measurements and saving to the files. Sync checkbox should be set when an external trigger or synchronization between boards is used. After that user can choose trigger type – differential or single-ended.

In a control section, there is a button for FPGA version read-back, a button for write settings into FPGA (settings are also automatically written when a measurement is starting), a button for setting DSP parameters, **button for setting new Bias value (Bias is not updated on measurement start – user need to set it manually)**, and connection status indicator.

The output section consists of a user-defined path for measurement saving, the Filename for measurements, the checkbox for making a new folder for each measurement series name, the checkbox for choosing file format (binary if unchecked, text if checked), the checkbox for saving files in *.zip archives, and a checkbox for automatically saving measurement data to file (or not if unchecked).

The application can connect multiple detectors at the same time and synchronize measured data between detectors. The readout boards matrix can be defined in the grid.xml file (for more information, please contact us). The status of each electronic board Ethernet connection is visible in the Settings tab in the main window. **Figure 8** shows this tab with unconnected and connected detectors.

a) b)

Figure 8 Data acquisition software V3.1 settings tab showing the readout boards matrix and Ethernet connection status: a) none of the readout boards is connected, b) all readout boards are connected

Using the Chart window, the user can online monitor signals from the detector. This is useful to check if everything works properly, how much flux we have from the X-RAY source etc. **Figure 9** shows the Data acquisition application charts window. This window has two tabs: Regular measurement and DSP. The regular measurement tab is used in Regular DAQ and Oscilloscope modes. This tab consists of two charts: a candlestick plot for all channels on the top and a channel line plot for one chosen channel. The channel for the line plot can be selected by "Channel nr" control. Charts can be auto-scaling and auto-updating or manual updating by the "Update" button. In DSP mode, data has a different form, so we use the second tab with a graph showing the deposited charge value for each channel separately.

a) b)

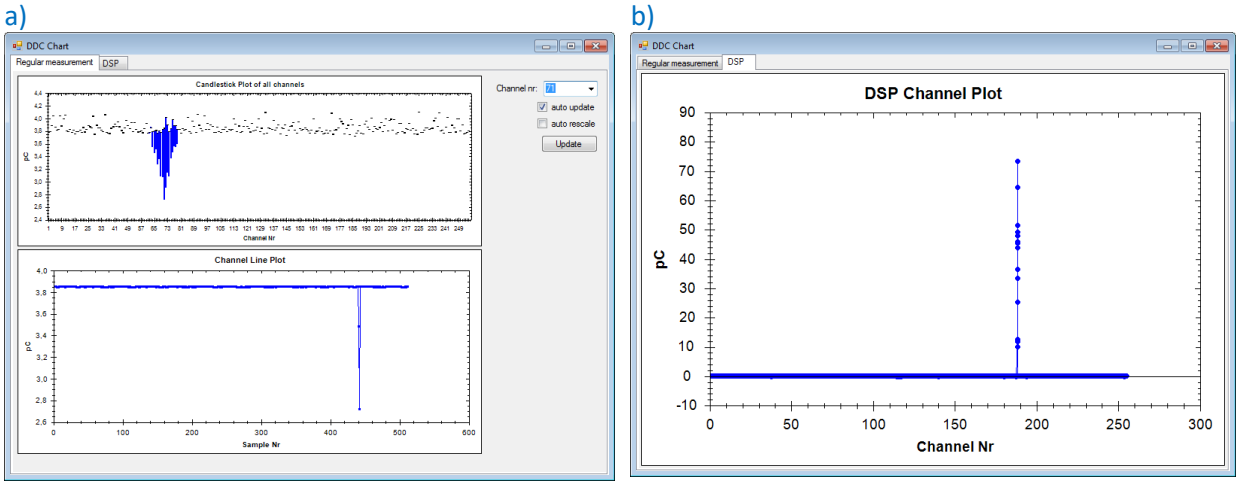


Figure 9 Data acquisition software V3.1 Chart window: a) Regular measurement tab, b) DSP tab

Obtained data can be saved in two different file types: text or binary. The former usually requires more disk space, but it can be easily analyzed; the second was designed to achieve the best save performance and lowest disk usage. The save process can be triggered automatically by software (if the autosave checkbox is checked) or manually by the user (using the save button).

Files are saved using the following name convention: measurmentName_index.dat, where the name can be set in the user interface, and the index is automatically set by software. In DSP mode, the saved file name convention is measurement Name_index_DSP.dat. A new folder can be created by the software for each new measurement name (if the proper option is chosen).

The regular measurements text file consists of two parts: header and data matrix. The header includes basic measurement settings (DDC range and integration time), data provided by the user (name, description), and resolution. Resolutions mean: how many channels (readout boards) are in the X and Y direction in the matrix. Files from the V3.1 application (for V2.0 readout) are not fully compatible with older ones (for 1.0 and 1.1. readouts).

Exemplary text file header:

```
#-------------DDC Params-------------#
# Range = 6,25 pC
# Integration time = 100
##-------------Other------------------##
## Name: test1
## Description:
## -
## Index: 0000
## Resolution: 256 x 0
```

The Data matrix begins with two lines. The first line contains numbers in a sequence where each number corresponds to sample No. The second line provides information about the time intervals between data samples - "1" means that data is consistent and data loss did not occur. The higher number e.g. "3", means that two samples were lost during transmission (it means that the time interval between samples is three times bigger). When there are few detectors in vertical arrangement (in grid.xml file), there is a third line with the same information as the second – that helps with data processing in visualization software.

After those lines start the NxM data matrix. When there is only one detector, or all of the detectors are in a horizontal line, then: N is fixed size and it's defined by the number of channels (number of readout boards times 256). M can vary and depends on container size (standard container size is 512 samples). The data structure in the file is as follows:

$$\begin{bmatrix} c_0 s_0 & \cdots & c_0 s_{M-1} \\ \vdots & \ddots & \vdots \\ c_{N-1} s_0 & \cdots & c_{N-1} s_{M-1} \end{bmatrix}$$

$c_N s_M -$ *channel* $\boldsymbol{n}$ *sample* $\boldsymbol{m}$

When the detectors matrix includes vertically positioned detectors, the matrix format is changed – every even line in the matrix contains data from vertical detectors. The data structure in a file is as follows:

$$\begin{bmatrix} c_{H0} s_0 & \cdots & c_{H0} s_{M-1} \\ c_{V0} s_0 & & c_{V0} s_{M-1} \\ \vdots & \ddots & \vdots \\ c_{HN-1} s_0 & \cdots & c_{HN-1} s_{M-1} \\ c_{VN-1} s_0 & & c_{VN-1} s_{M-1} \end{bmatrix}$$

$c_{HN} s_M -$ *channel* $\boldsymbol{n}$, *sample* $\boldsymbol{m}$, *channels in horizontal arrangement*
$c_{VN} s_M -$ *channel* $\boldsymbol{n}$, *sample* $\boldsymbol{m}$, *channels in vertical arrangement*

DAQ mode text file also consists of two-part: header and data matrix. The header is very similar to Regular, but it contains additional information such as IQD threshold value, Peak width, and Trig Threshold value. DSP files from the V3.1 application (for V2.0 readout) are not compatible with older ones (for 1.0 and 1.1. readouts).

Exemplary text file header:

```
#------------DDC Params------------#
# Range = 6,25 pC
# Integration time = 100
##------------Other-----------------##
## Name: test1
## Description:
## -
## Index: 0000
## Resolution: 256 x 0
##------------DSP--------------------##
# IQD treshold = 5
# Peak width = 10
# Trig Threshold = 1,00020000
##------------Data--------------------##
```

In this mode, data are in form of a table with three columns. The first line contains parameter names, such as Charge, Peak Center, and Frame number. After the first line, there are numerical data divided into

three columns. Every row is a single detected event with peak parameters. The length of this file depends on the measurement number selected in the application.

The software uses the "," as a decimal mark symbol (independently from the decimal mark used in the operating system). Data samples are separated by tabulator "\t". Each row is ended by a new line mark. Binary file specification has been described in **Table 8**.

Table 8 Binary file specification

Position	Type	Name	Description
1	B	Range	0 to 3 value corresponding to DDC range (see datasheet)
2	UINT	Integration time	Time in µs
3	UINT	Channel number	Number of channels - in current hardware solution – 256
4	UINT	Sample number	Number of samples obtained for single-channel
5	UINT	Dt	Sample number-1 values corresponding to time different between samples (as in text file)
6	DOUBLE	Data matrix	-

Data alignment is the same as in text format file (see data matrix), but samples are not separated by tabulator. Binary types definition has been described in **Table 9**.

Table 9 Binary types definition

Type	Description
B	8-bit unsigned integer
UINT	32-bit unsigned integer
DOUBLE	double-precision floating-point format - 64 bit

6. PC software – data visualization

This application is intended for the visualization of data gathered by the GEM detector. The program works with collected raw data and processes them to display a final image. With that software, it is also possible to remove so-called "hot pixels" from the image, plot the energy spectrum of the detected events, filter the energy range of the events that are taken into account during the reconstruction and plot the distribution of events over time. The application consists of four tabs: the main one, on which the reconstructed image is displayed, tab with a graph showing the energy spectrum, tab with a graph of the distribution of the number of events in time, and bookmarks with settings. **Figure 10** shows screens from visualization software.

More information about visualization software and our detector you can find here:
http://techtra.pl/en/technology/gem-based-detector/

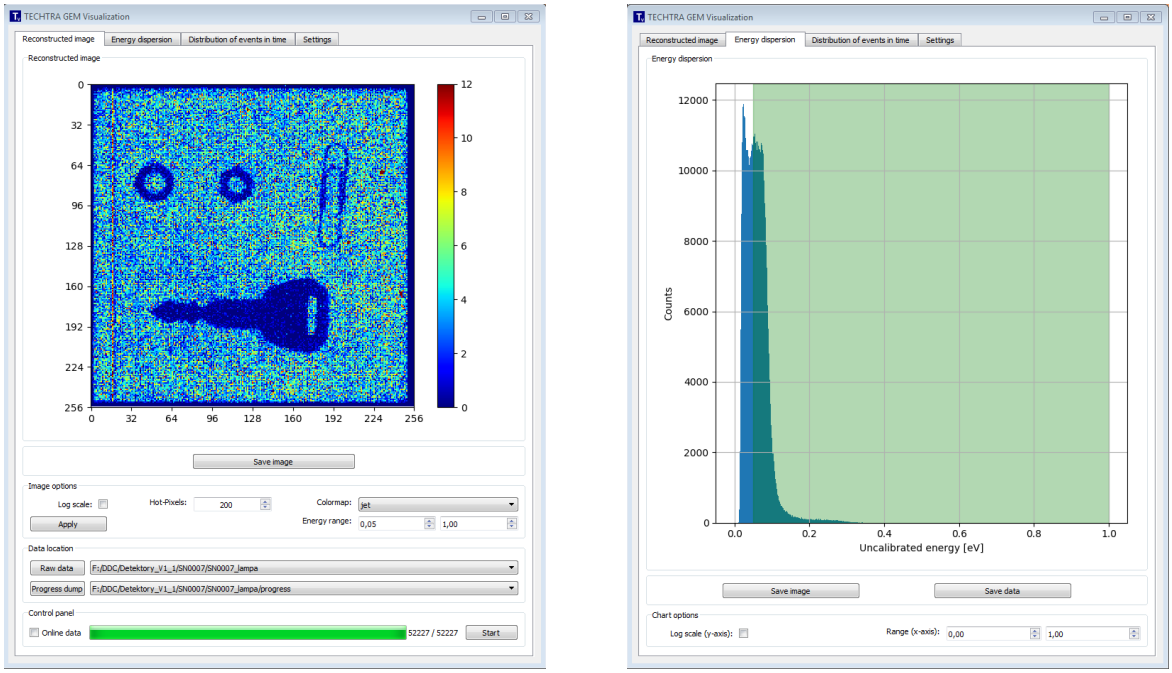


Figure 10 Data Visualization software